IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

OPTi, Inc.	§	
	§	**CIVIL ACTION 2:07-cv-00021 (CE)**
Plaintiff,	§	
	§	**JURY**
vs.	§	
	§	
Apple Inc.	§	
	§	
Defendant.	§	

APPLE INC.'S RENEWED MOTION FOR JUDGMENT AS A MATTER OF LAW
AND
MOTION FOR A NEW TRIAL REGARDING 35 U.S.C. § 112 DEFENSE

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I. INTRODUCTION

Apple renews its request for judgment as a matter of law, and alternatively requests a new trial, on its defense that the asserted claims of U.S. Patent No. 6,405,291 ("the '291 patent") are invalid pursuant to 35 U.S.C. § 112. As set forth below, Apple's requests are based on the '291 specification's failure to describe and enable the full scope of claims 73, 74, and 88—the only remaining asserted claims in this case.[1]

Ensuring that patentees do not, through overly-broad claim drafting, extend their patent monopoly beyond that which they actually invented and contributed to the public knowledge through their patent disclosure is a fundamental purpose of the enablement requirement of 35 U.S.C. § 112. Federal Circuit precedent repeatedly and consistently emphasizes the policy underlying this critical intersection of disclosure and claim scope in a steady line of cases invalidating broad patent claims exceeding the scope of what is enabled in the specification, most recently in *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008) (citation omitted):

> The rationale for this statutory requirement is straightforward. Enabling the full scope of each claim is 'part of the *quid pro quo* of the patent bargain.' A patentee who chooses broad claim language must make sure the broad claims are fully enabled.

In this case, OPTi vigorously argued for and received a claim scope by which its "constant rate" limitation was construed to cover what its own inventor and expert admit it *did not* invent or enable—a completely different chipset architecture capable of data transfers at 100% of the maximum PCI throughput.

The impact of OPTi's overreaching claim scope pervaded the trial. Even after OPTi's

[1] This motion addresses only Apple's Section 112 defense, which was not resolved by the jury verdict. Apple will file a separate motion for judgment as a matter of law and a new trial concerning willfulness, anticipation, obviousness, and damages.

inventor and expert unequivocally admitted at trial that OPTi did not invent, teach, disclose or enable a chipset architecture for achieving a 100% PCI throughput, OPTi presented the jury with a damages theory seeking to capture *precisely* the alleged value of the performance benefit *neither* invented *nor* enabled by the OPTi inventors (132MB/sec, or 100% of the maximum PCI throughput) over what they *did* invent and try to enable (67MB/sec, or 50% of the maximum PCI throughput). Indeed, that very performance differential was the *only* basis of OPTi's damage claim, since its theory presumed that Apple could achieve 67MB/sec without using the alleged invention.[2]

OPTi mistakenly believes that so long as the '291 patent discloses and enables *one* "constant rate" design (one that achieves a constant rate by uniformly inserting delays), it has sufficiently enabled a claim that extends to *all* possible "constant rate" designs (including those that are "constant" only by the virtue of a different architecture designed to avoid delays altogether). OPTi's flawed argument has been repeatedly and unequivocally rejected by Federal Circuit precedent. Patent claims *can no doubt be* enabled by description of a single embodiment, but only so long as that one embodiment enables the full scope of the claims, and a patentee is not required to describe every known, conceivable, or possible embodiment within that scope. But this cannot save OPTi's claims. The salient point here is that whether through a description of one, two or a dozen embodiments, a patentee must nonetheless enable the *full scope* of what is claimed. Contrary to OPTi's argument, therefore, "a patentee cannot always satisfy the

[2] OPTi's inventor admitted that the design described in the '291 patent could only achieve the 50% rate, not the 100% rate (Ex. 1, Trial Tr. Apr. 17, 2009 P.M. Session, p. 13:11-17 (Ghosh)) and that it could achieve only 66MB/sec (*Id*. pp. 15:23-16:2 (Ghosh)). OPTi's expert repeatedly confirmed that Apple could achieve 67MB/sec without using the invention. (Ex. 2, Trial Tr. Apr. 20, 2009 A.M. Session, pp. 105:1-13, 117:18-118:5, 125:19-23 (Smith).) Hence, the value of "improved performance" that OPTi's damage claim sought to capture was *solely* the value of the 100% zero wait state design over what could be achieved by either Apple without the invention or by OPTi with its own design as described in the '291 patent.

requirements of section 112, in supporting expansive claim language, merely by clearly describing one embodiment of the thing claimed." *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1346 (Fed. Cir. 2005).

Compliance with Section 112 is a question of law based on underlying facts, and in this case, all of the relevant underlying facts are undisputed. Thus, although the Court did not submit Apple's 112 defenses to the jury, there was no genuine dispute for the jury to decide. As the Federal Circuit remarked when it affirmed invalidity of claims that a patentee asked to be construed more broadly than what the patentee actually invented and enabled, "[t]he motto 'beware of what one asks for,' might be applicable here." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 481 F.3d 1371, 1380 (Fed. Cir. 2007). OPTi asked for and received a broad claim scope in order to cover that which it admittedly did not invent or teach (and which it could not have taught, since it admittedly did not know how to make full-speed design at the time of the '291 filing), violating the *quid pro quo* of the patent bargain. It must now live with the consequences, and JMOL of invalidity is required.

II. ARGUMENT

A. Legal Standard for JMOL.

JMOL is appropriate where "the court finds that a reasonable jury would not have a legally sufficient evidentiary basis to find for the [non-movant] on that issue." Fed. R. Civ. P. 50(a)(1). The court must "determine whether viewing the evidence in the light most favorable to the non-moving party, and giving the non-movant the benefit of all reasonable inferences, there is sufficient evidence of record to support a jury verdict in favor of the non-movant." *Ericsson, Inc. v. Harris Corp.*, 352 F.3d 1369, 1373 (Fed. Cir. 2003) (internal quotations omitted) (quoting *Southwest Software, Inc. v. Harlequin Inc.*, 226 F.3d 1280, 1289 (Fed. Cir. 2000)).

"Whether a claim satisfies the enablement requirement of 35 U.S.C. § 112, ¶ 1 is a

question of law, reviewed de novo, based on underlying facts, which are reviewed for clear error." *Sitrick*, 516 F.3d at 999. Here, where none of the underlying facts are in genuine dispute, enablement collapses into a question of law appropriate for the Court to decide.

B. Apple is Entitled to JMOL of Invalidity under 35 U.S.C. § 112.

1. Because OPTi sought and received a broad claim scope covering a 100% speed, zero-wait-state design that *eliminates delays*, it was required to enable that full scope, not merely a single embodiment that meets the claim requirements by *inserting delays* to achieve 50% speed.

"[A]s part of the *quid pro quo* of the patent bargain, the applicant's specification must enable one of ordinary skill in the art to practice the full scope of the claimed invention." *AK Steel Corp. v. Sollac & Ugine*, 344 F.3d 1234, 1244 (Fed. Cir. 2003). Thus, a patentee cannot always support a broad claim by describing only a single embodiment:

> To hold otherwise would violate the Supreme Court's directive that '[i]t seems to us that nothing can be more just and fair, both to the patentee and the public, than that the former should understand, and correctly describe, just what he has invented, and for what he claims a patent.' *Merrill v. Yeomans*, 94 U.S. 568, 573-74 (1876). *. . . Thus, a patentee cannot always satisfy the requirements of section 112, in supporting expansive claim language, merely by clearly describing one embodiment of the thing claimed.*

LizardTech, 424 F.3d at 1346 (citations omitted) (emphasis added).

Numerous and recent Federal Circuit precedent that is directly on point demonstrate that JMOL here is appropriate, including *Liebel-Flarsheim, Auto. Techs. Int'l, Inc. v. BMW of N. Am., Inc.*, 501 F.3d 1274 (Fed. Cir. 2007), *AK Steel, Nat'l Recovery Techs., Inc. v. Magnetic Separation Sys., Inc.*, 166 F.3d 1196 (Fed. Cir. 1999), *Sitrick*, and *LizardTech*. This precedent sets forth the legal standards for the enablement question at issue here, and exemplify how and why the Federal Circuit has repeatedly and consistently rejected the faulty arguments that OPTi has signaled it will make to save its patent.

Invalidity for lack of enablement is a conclusion of law based on clear and convincing

proof of underlying facts. *Liebel-Flarsheim*, 481 F.3d at 1377. While disclosure of a single embodiment can enable a broad claim in circumstances where results are predictable and within the ordinary knowledge in the art, the same is not true where the single disclosed embodiment does not permit one skilled in the art to make and use the invention as broadly as it was claimed. *Id.* at 1379-80 (disclosure of a single embodiment, an injector system with a pressure jacket, did not permit one skilled in the art to make and use the invention as broadly as it was claimed, including without a pressure jacket, particularly where the specification effectively taught away from a jacketless design by electing and enabling the design with the jacket).[3] The rule that a specification need not disclose what is well known in the art is merely a rule of supplementation, not a substitute for a basic enabling disclosure. *Auto. Techs.*, 501 F.3d at 1283. The omission of minor details does not cause a specification to fail to meet the enablement requirement. But when there is no disclosure of any specific starting material or of any of the conditions under which a process can be carried out, however, undue experimentation is required. *Id*. at 1283-84.

In this case, where the scope of a claim is construed to include two different modes of an invention, one of which is taught and enabled, and the other of which had not been figured out by the inventor himself and could not be implemented by one of ordinary skill in the art based on the teachings of the specification, the claim will be invalid for lack of enablement. *See Auto. Techs.*, 501 F.3d at 1283-85. (affirming invalidity for lack of enablement where the scope of the claims (requiring "sensors") was construed to include not only mechanical sensors, but also electronic sensors; the specification disclosed the concept of using electronic sensors, but the

[3] *See also AK Steel*, 344 F.3d at 1244 ("That is not to say that the specification itself must necessarily describe how to make and use every possible variant of the claimed invention, for the artisan's knowledge of the prior art and routine experimentation can often fill gaps, interpolate between embodiments, and perhaps even extrapolate beyond the disclosed embodiments, depending upon the predictability of the art. . . . But it does mean that, when a range is claimed, there must be reasonable enablement of the scope of the range.") (citations omitted).

patentee did not disclose the architecture required for achieving the electronic sensor design and did not enable one of skill in the art to achieve such a design based on what was disclosed).[4]

When a "range" of modes is within the scope of a broad claim, "there must be reasonable enablement of the scope of the range." *AK Steel*, 344 F.3d at 1244.[5] Testimony of an inventor that he did not himself know how to achieve the mode of invention not taught in the specification will also support a finding that the claim was not enabled. *Nat'l Recovery*, 166 F.3d at 1198 (affirming invalidity for non-enablement where inventor testified that as of the patent filing date, the patentee "'did not know particularly how to do that …. [and was] still developing that process.'").

2. After arguing to the PTO, the Court, and jury that the novel aspect of the broad '291 claims was the ability to achieve zero wait state performance, OPTi must enable that scope.

a. OPTi argued to the PTO that the ability to transfer data "with no wait states" was a "substantial benefit" that distinguished the claimed '291 invention from the VIA prior art.

There is no dispute that the asserted claims of the '291 patent, as construed at OPTi's urging, include within their scope the "zero wait state" design that OPTi did not teach or know how to do when the patent was filed. In fact, when OPTi affirmatively argued that very claim scope before the PTO based on its "constant rate" claim element in order to distinguish the prior

[4] Notably, the Court in *Auto. Techs.* ended its analysis by pointing out the same irony that it had noted in *Leibel*, namely that the patentee itself sought to have the scope of the claims of the patent include both mechanical and electronic side impact sensors—"It succeeded, but then was unable to demonstrate that the claim was fully enabled. Claims must be enabled to correspond to their scope." *Auto. Techs.*, 501 F.3d at 1285.

[5] *See also Sitrick,* in which the claims at issue, at the patentee's request, were construed broadly to cover both movies and videogames, but the specification disclosed only a videogame embodiment. *Sitrick*, 515 F.3d at 1000. The Federal Circuit affirmed summary judgment of invalidity for lack of enablement. *Id*. at 1002. Similarly, in *LizardTech*, the Federal Circuit affirmed summary judgment of invalidity under 35 U.S.C. §112, where a patent claim covered *all* ways of making a seamless DWT, but the specification described only one way, and persons of ordinary skill in the art would not have been able to make a seamless DWT in the alternative way based on the teachings of the specification. *LizardTech*, 424 F.3d at 1345-46.

art, OPTi established a point of novelty that it was then *required* to fully describe and enable in the specification. It was not enough for OPTi to enable a narrow, limited mode of the design and then argue that one of skill in the art could have figured out a different design that was not described or enabled. When the mode of a claimed invention that is *not* taught in the patent specification is touted as a "novel aspect of the invention," the patentee *cannot* then simply "state that known technologies can be used" to create that design. *Auto. Techs.*, 501 F.3d at 1283 ("Given that the novel aspect of the invention is side impact sensors, it is insufficient to merely state that known technologies can be used to create an electronic sensor.").

OPTi violated that fundamental principle. During the prosecution of the '291 patent, OPTi argued that a prior art chipset, the VIA VT82C505, did not anticipate because it failed to transfer data on *every single clock cycle* (at 100% of the PCI bus bandwidth) across multiple lines. The VIA VT82C505 chipset was much faster than the 50% rate chipset that OPTi disclosed in the '291 patent. According to timing diagrams that OPTi submitted to the PTO, the VT82C505 transferred data in 100% constant rate bursts: "This figure [of a VT82C505 in action] shows a PCI master read with a host data rate which is fast enough to sustain the zero-wait-state data transfer across the PCI bus." (Ex. 3, Excerpt from the '291 Patent's File History regarding OPTi's Request for Further Consideration of IDS Documents D2-1 through D2-7, Document D2-4, PTX 462 at OPTIAPPLE 153245.)

Although the VIA timing diagrams showed zero wait state transfers across multiple lines, OPTi argued that the VT82C505 could not sustain zero wait transfers forever. OPTi proclaimed that its '291 patent, in contrast to VIA, provided the "substantial benefit" of *continuous* data transfers "with no wait states between the data unit transfers":

> ***One of the substantial benefits*** that are facilitated by aspects of Applicants' invention, is that if the predictive snoop access is

> performed early enough during a cache line transfer, and as long as snoop accesses do not trigger a cache writeback cycle, then data transfer can continue across cache line boundaries without any additional delay. ***For example, if the system transfers data to the PCI-bus master with no wait states between data unit transfers (i.e. at a rate of one data unit transfer per PCI-clock), then nor will any wait states be required between the last data unit of one cache line and the first data unit of the next cache line***….

(Ex. 3, Excerpt from the '291 Patent's File History regarding OPTi's Request for Further Consideration of IDS Documents D2-1 through D2-7, PTX 462 at OPTIAPPLE 153202 (emphasis added).) OPTi contended that VIA's chipset, unlike OPTi's '291 invention, could not sustain 100% data rate for more than three lines, and would eventually insert a single wait state, briefly interrupting the transfers:

> Given all the logic delays inherent in a determination of whether to negate /TRDY in response to HITM* or to leave it asserted, plus the requirement in the PCI-bus specification for /TRDY to be stable a certain amount of time *before* each PCI-bus rising edge (called the setup time), plus additional margin required by good engineering practice, Applicants believe that it would be extremely unlikely that the VT82C505 would leave /TRDY asserted for the first PCI-clock rising edge after the last data transfer of the second cache line. ***Instead it would automatically insert a wait state, in order to allow sufficient time to safely and reliably determine whether it needs to stop or delay the transaction in response to HITM*. A wait state would mean that the VT82C505 did not maintain a constant data transfer rate across the second cache line boundary.***

(Ex. 3, Excerpt from the '291 Patent's File History regarding OPTi's Request for Further Consideration of IDS Documents D2-1 through D2-7, PTX 462 at OPTIAPPLE 153208 (bold and italic emphasis added).)

Thus, OPTi contended that the novel aspect of the claimed '291 invention over the VIA prior art was the ability of the '291 invention *to sustain zero wait state performance over multiple lines*. Significantly, OPTi did not argue that the VIA chipset was unable to perform the slower 50%, every other clock cycle transfer disclosed in the '291 patent. (By virtue of PCI

compliance, chipsets must be able to slow down and insert wait states.[6]) Instead, OPTi argued that the VIA chipset could not sustain 100%, zero-wait state transfers for more than two lines, and would eventually need to insert at least one wait state into the transfer. After arguing that the claims were novel over the prior art because they provided for sustained 100%, zero wait state data transfers, OPTi was obligated to provide enabling support for its broad claim. "[T]he novel aspect of an invention must be enabled in the patent." *Auto. Techs.*, 501 F.3d at 1283. OPTi's specification indisputably teaches only the design that uses every other clock cycle, and not the zero wait state design that eliminates those delays, and the asserted claims are therefore invalid.

b. At *Markman*, summary judgment, and trial, OPTi argued that the '291 invention, unlike the prior art, provided 100% rate, zero wait state transfers.

In litigation, OPTi continued to argue that the claimed '291 invention, unlike the prior art, provided 100% rate, zero wait state data transfers across multiple lines. First, OPTi successfully argued for a sweeping construction of the "constant rate" term that would cover the *entire range* of possible "constant rates," up to and including a 100% rate.[7] OPTi also

[6] The PCI Specification provides that a PCI device (which can be either a "target" or "master") must be able to insert wait states by de-asserting the IRDY# or TRDY# signals, and must be able to respond to a wait state inserted by the other end of the PCI transaction. (Ex. 4, PCI Local Bus Specification, Revision 2.0, Apr. 30, 1993, DX 64 at OPTIAPPLE at 139190.) Thus, by virtue of being PCI compliant, the VIA chipset had the ability to insert wait states, and could slow down to 50% performance, if for some reason the application wished it to do so.

[7] The Court adopted OPTi's construction of "constant rate" in the co-pending *AMD* case, and the parties yielded to the Court's construction in this case as well. AMD contended that "constant rate" meant: "The same number of wait states is inserted between the transfer of each data unit, without inserting any additional wait states." AMD's proposed construction of "constant rate" would have limited the claims to rates of 50% or less, and would have been supported by the OPTi specification. OPTi argued for a broader construction that would cover *any* "constant rate," contending that "if the inventors had wanted to limit the claims to transfers with a particular allocation of wait states, they could have done so." (Ex. 5, PLAINTIFF OPTI INC.'S REPLY *MARKMAN* BRIEF PURSUANT TO P.R. 4-5(c), Dkt No. 74 pp. 6-7, Civil Action No.: 2:06-CV-00477 CE (June 25, 2008).) The Court adopted OPTi's construction, and applied it

successfully argued for a construction of "one and only one snoop access" of the cache memory during transfer of a line that broadened the claim to cover a design which pre-fetched (and snooped) *multiple* lines ahead during the transfer of a single line (requiring multiple snoop accesses of the cache memory during that transfer), even though the specification described neither the architecture nor the aspiration to do so.[8] Next, OPTi obtained summary judgment of infringement by proving that Apple's products performed multi-line bursts at the 100% rate (zero wait states). Finally, at trial, OPTi's damages presentation repeatedly argued that OPTi was entitled to damages for the value of the 100% rate transfers as compared to 50% rate transfers, and contended that the '291 patent ensured that the PCI bus is "kept *full of traffic* flowing at a constant rate from one place to another." (Ex. 9, Trial Tr. Apr. 17, 2009, A.M. p. 29:12-15 (OPTi's opening statement).)

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both to the *AMD* case and to this litigation.

[8] In light of OPTi's testimony at trial, OPTi cannot continue to imply that the references in the specification to "buffers" somehow show that the patent teaches multiple line pre-fetching or snooping ahead multiple lines. Moreover, although the order granting summary judgment of infringement noted that "the specification contemplates the use of buffers and a buffer controller in the chipset. '291 patent, at 9:39-42." (Ex. 6, Memorandum Order, Dkt No. 132 p. 3 (Apr. 3, 2009).), that structure must not be confused with the type of structure necessary to achieve 100% rate transfers. To the contrary, the reference to the "data buffer controller" in the '291 patent is a reference to the 556 chip in the OPTi Viper chipset, which is indisputably not a multi-line prefetch buffer and is not able to accomplish 100% rate, zero wait state transfers, as admitted by inventor Ghosh at trial. (Ex. 7, Trial Tr. Apr. 22, 2009 A.M. Session, pp. 52:13-17, 90:9-22, 91:4-10 (Ghosh) (testifying that the "patent doesn't teach zero wait state performance because it doesn't have multiple lines of buffering").) In fact, the "data buffer controller" 556 chip provided a latch for *one single 32 bit data unit*. A single data unit buffer is not a multi-line prefetch buffer, and thus, cannot possibly be used to prefetch lines and perform zero wait state transfers. The '291 "buffer" structure, combined with OPTi's decision to separate the 556 chip from the 558 chip, contributed to the Viper chipset's awkward and slow data transfer sequence, which could achieve no more than 50% of the PCI bandwidth. (*See* Ex. 8, '291 patent, at OPTIAPPLE 089897 col. 13:60-14:24 (describing the transfer sequence).) Thus, the "buffer" and "buffer controller" cited in the patent at column 9 did not teach or enable how to make a zero wait state chipset—to the contrary, those structures were part of an architecturally flawed design that would have led persons of ordinary skill in the art down the primrose path to a half-speed product.

3. At trial, OPTi conceded that the '291 patent describes and enables only a chipset that is limited to the 0-50% rate, and does *not* enable zero wait state transfers.

After successfully arguing to the PTO, the Court, and the jury that the claimed invention, unlike the prior art, provided the "substantial benefit" of "no wait state" transfers across many lines, OPTi finally had to substantiate its claims at trial. To support the broad claims to the entire range of possible "constant rates," OPTi needed to provide enabling disclosure of the *full scope* of that claimed invention. The law did not require OPTi to disclose *every* possible way of achieving a zero wait state design. But because OPTi's "constant rate" claims cover the entire possible range of rates, including the 100% rate, the law required OPTi to enable *at least one way* to achieve that claimed range.

It is undisputed that OPTi did not meet that standard. OPTi's own expert, Dr. Smith, expressly admitted that OPTi did not describe or enable *any* embodiment able to achieve a 100% rate. To the contrary, OPTi described only a single chipset, the Viper, with a fundamental architectural limitation that restricted the design's bandwidth to no more than a 50% rate. The evidence also established beyond dispute that persons of ordinary skill in the art, armed with OPTi's '291 patent and seeking to achieve the full range of claimed "constant rates" could not have achieved a 100% rate, zero wait state design without undue experimentation.

All of the technical witnesses—inventor Ghosh, OPTi's expert, and Apple's expert—agreed that the '291 specification describes a limited system only able to transfer data at a low range of rates, between 0-50% of the maximum PCI rate. The OPTi inventors, who were trying to develop OPTi's first-ever PCI chipset, embraced the 50% "constant rate" concept initially not as a proxy for speed or performance, but as a modest, achievable design target—"the valuable part of having a constant rate transfer was simply the ease of design." (Ex. 1, Trial Tr. Apr. 17, 2009 P.M. Session, p. 18:16-19 (Ghosh).) Ghosh acknowledged that maintaining a "constant

rate" was not valuable in and of itself to the user—a "user would look at throughput, not whether the transfer rate was constant or not." (Ex. 1, Trial Tr. Apr. 17, 2009 P.M. Session, pp. 18:12-15, 16:20-24 (Ghosh) ("constant rate has nothing to do with speed itself"); *see also* (Ex. 10, Trial Tr. Apr. 21, 2009, A.M. Session, p. 70:11-23 (Colwell).)

Because Ghosh and Tung adopted only a modest goal of a 50% rate design—not a fast one—they constructed a design that had a fundamental, inherent architectural limitation. Their design, described in the '291 patent, used a three-chip architecture, without any multi-line prefetch buffering. (Ex. 7, Trial Tr. Apr. 22, 2009 A.M. Session, p. 91:4-10 (Ghosh).) The design allowed OPTi to rush the chipset into production in early 1995, but restricted its PCI performance to a maximum 50% rate. As Ghosh testified: "The architecture we initially settled to *did not allow us to go to maximum throughput*." (Ex. 9, Trial Tr. Apr. 17, 2009 A.M. Session, p. 113:1-9 (Ghosh) (emphasis added); Ex. 7, Trial Tr. Apr. 22, 2009 A.M. Session, pp. 52:13-17, 90:9-22, 91:4-10 (Ghosh) (testifying that the "patent doesn't teach zero wait state performance because it doesn't have multiple lines of buffering").)

The architectural limitation allowed OPTi to launch its first PCI-compatible chipset in early 1995, but hindered performance so severely that the OPTi chipset design was on the verge of obsolescence even before Ghosh and Tung filed the '291 patent application. Product reviewers noted that the three-chip Viper "system architecture is not as straightforward as that of other chip sets" and observed that the Viper's "PCI performance is relatively poor" compared to Intel's and VIA's competing products. (Ex. 11, Yong Yao, *Vendors fight for Pentium core-logic market; Intel is king of the land, most others are losing chip-set share*, Microprocessor Report, Aug. 21, 1995, DX 1278 at OPTIAPPLE 110277.)

Several months after the product launch, OPTi filed the '291 specification, disclosing the

impaired Viper design. Ghosh testified that when he filed the '291 application, a zero wait state design was still merely in the "concept phase" at OPTi, and he had simply not "figured out" how to achieve rates greater than 50%.

> Q: Okay. Well, as of the time that you filed the application for the '291 patent, you had, in fact, not yet figured out how to practice the invention to achieve a zero wait state performance, had you?
>
> A: I don't think so.
>
> . . .
>
> Q: Now, do you recall that, in fact, as of July 1995, that you had not, in fact, figured out how to practice the invention to achieve the zero wait state performance?
>
> A: Yes. It was in the concept phase, as it says.

(Ex. 1, Trial Tr. Apr. 17, 2009 P.M. Session, pp. 10:17-21; 13:6-10 (Ghosh).)[9]

> Q. You agree that your patent does not disclose how to achieve a zero wait state performance, right?
>
> A. Right.

(Ex. 7, Trial Tr. Apr. 22, 2009 A.M. Session, p. 90:20-22 (Ghosh).)

The experts for both sides analyzed the '291 patent and concluded that it did not enable 100% rates. Apple's expert, Dr. Colwell, testified that the '291 patent did not show how to use the full PCI bandwidth. (Ex. 10, Trial Tr. Apr. 21, 2009 A.M. Session, p. 71:1-3 (Colwell).) OPTi's expert, Dr. Smith, also conceded the issue, agreeing that the '291 patent did not enable 100% rate, or zero-wait state performance:

> Q. Sure. In your opinion, the pre-snoop patent did not enable zero wait state transfers; isn't that correct?

[9] The '291 patent's only mention of full rate transfers is a cursory statement that "[i]n another embodiment of the present invention, a wait state may not be necessary." (Ex. 8, '291 Patent, DX 2 at OPTIAPPLE 089897 col. 14:17-18.) Not only does this statement fail to provide any enabling description, it fails to say that such a mode is possible, offering only that a no-wait-state implementation "may" be achievable. (*Id.*)

A. That's correct.

(Ex. 12, Trial Tr. Apr. 22, 2009 P.M. Session, p. 98:6-9 (Smith).) Dr. Smith's admission, by itself, is dispositive. OPTi made no effort to redirect Dr. Smith on the issue, or to qualify his unambiguous admission. As OPTi's expert on validity, Dr. Smith carefully considered and analyzed the patent and testified, under oath, that OPTi's patent "***did not enable***" zero wait state transfers. No reasonable jury could disagree.

Not only are Dr. Smith's testimony, Ghosh's testimony, and Dr. Colwell's testimony enough to require the requested JMOL, but the record also establishes that achieving a 100% rate, zero wait state with a chipset from the '291 patent's description would have required undue experimentation. Indeed, there was *no* evidence in the record to support a contrary conclusion. Dr. Smith went to great lengths to show that achieving at 100% rate was difficult even when a highly skilled firm—such as Compaq—started with the *correct* chipset architecture. (Ex. 12, Trial Tr. Apr. 22, 2009 P.M. Session, pp. 51:17-65:24 (Smith).) Dr. Smith never recanted his statement that the '291 patent did not enable zero wait state transfers, or offered any opinion or analysis as to how one of skill in the art could make the leap from OPTi's restrictive architecture to a zero wait state design. Similarly, OPTi emphasized that although VIA's chipset could achieve a 100% rate for a while, it could not sustain it over three or more lines. (Ex. 3, Excerpt from the '291 Patent's File History regarding OPTi's Request for Further Consideration of IDS Documents D2-1 through D2-7, PTX 462 at OPTIAPPLE 153202-203, 153206-211.) Moreover, as Intel designer Brian Langendorf testified, Intel concluded that trying to take an *existing* architectural design and change it to a 100% rate chipset would have been "quite complex, and it was one of those situations where retrofitting it into an existing design would have been far more work and risk than just doing it from scratch." (Ex. 7, Trial Tr. Apr. 22, 2009 A.M. Session, p. 120:21-25 (Langendorf).) Finally, OPTi itself later moved away from the '291 design and

embraced a single-chip design, with multiline prefetch buffers, to achieve zero wait state, 100% rate transfers. In the first quarter of 1997, over a year after the filing date of the '291 patent, OPTi announced volume shipments of its new single-chip solution, the "FireStar," which had "deep buffering features" to "improve system performance." (Ex. 13, OPTi's 1996 Annual Report, DX 960 at OPTIAPPLE 021533.)[10]

4. Because the '291 claims sweep far beyond the range that OPTi described and enabled, the '291 claims are invalid.

"The scope of the claims must be less than or equal to the scope of the enablement." *Nat'l Recovery*, 166 F.3d at 1196. The record irrefutably establishes that OPTi described and enabled a chipset that could transfer data no faster than the 50% rate—the architecture prohibited the chipset from going any faster—and that OPTi did not know, when it filed the '291 application, how to exceed the 50% ceiling and achieve a 100% rate, zero wait state design. Nevertheless, OPTi urged the Court to construe the claims to cover the entire possible range of "constant rates," including the zero wait state, 100% rate that was nothing more than an elusive "concept" to OPTi's engineers at the time of filing. OPTi then went on at trial to capture the value of achieving the 100% rate over the inferior 50% rate, even though OPTi itself did not know, much less teach in its specification, how to achieve the superior rate. This case is "a classic example of a claim that is broader than the enablement as taught in the specification." *Nat'l Recovery*, 166 F.3d at 1196.

OPTi argues that it enabled claims to the entire "constant rate" range because the specification taught at least one example in that range, a 50% rate. OPTi's "one embodiment is enough" argument misstates the law of enablement and is contrary to long-established Federal

[10] An OPTi representative, Mr. Mazzoni, testified that the FireStar did not use the Viper's three-chip architecture and was able to achieve a faster rate. (Ex. 1, Trial Tr. Apr. 17, 2009 P.M. Session pp. 48:23-49:11 (Mazzoni).)

Circuit precedent. A single embodiment is sufficient only when that embodiment enables the full scope of the claims to a person of ordinary skill in the art. But due to a fundamental architectural restriction and the absence of multiline prefetch buffering, the *only* embodiment that OPTi described in the '291 patent could not achieve the 100% rate that formed the basis of OPTi's damages case. Consequently, the '291 patent failed to enable the full scope of the claims, and the claims are invalid.

C. In the Alternative, Apple is Entitled to a Trial on Enablement.

The material facts are undisputed: (1) the '291 patent claims a "constant rate" range including a zero wait state, 100% rate, (2) as Dr. Smith conceded, the '291 patent did not enable a zero wait state, 100% rate, (3) the OPTi inventors did not know how to achieve a 100% rate, which was only a "concept" to them when they filed the application, and (4) the '291 patent describes a restrictive architecture, without the necessary deep prefetch buffers, that could not achieve the zero wait state, 100% constant rate without extensive redesign and undue experimentation. Judgment as a matter of law of invalidity under 35 U.S.C. § 112 is required.

Even if OPTi were able to raise a dispute of material fact—and it cannot—Apple is at a minimum entitled to a trial on its enablement defense. A reasonable jury, properly instructed, could have found the claims invalid for failure to comply with 35 U.S.C. §112. Consequently, if the Court does not enter JMOL of invalidity, Apple is entitled to a new trial on the issue. *Hartsell v. Doctor Pepper Bottling Co.*, 207 F.3d 269, 272 (5th Cir. 2000) (noting that a new trial is required unless, "based upon the entire record . . . the challenged instruction could not have affected the outcome of the case").[11]

[11] Apple's pretrial jury instructions included the enablement issue, and the Pretrial Order included enablement as well. Both sides moved for JMOL on the defense, on the grounds that none of the factual issues were in dispute, and the defense distilled to a single legal question. When the Court at the charge conference indicated that it was carrying the cross-motions for

III. CONCLUSION

The record is undisputed. As Dr. Smith conceded, the '291 patent claims the entire range of "constant rate" transfers, including a 100% rate, but the '291 patent does not enable the full scope of the claimed invention. Instead, the '291 patent disclosed only a chipset with severe architectural limitations, restricted to a 50% rate. OPTi's inventors did not know how to exceed the 50% rate, and persons of ordinary skill in the art, armed with OPTi's patent, would have been forced to undergo extensive experimentation and new design work to achieve the 100% rate. JMOL of invalidity, or in the alternative a new trial on Apple's section 112 defense, is required.

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Respectfully submitted,

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JMOL, Apple requested that the enablement issue be submitted to the jury, with an instruction that the claims must enable the full scope of the claimed invention. (Ex. 14, Trial Tr. Apr. 23, 2009 A.M. Session p. 6:10-23 (charge conference).)

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CERTIFICATE OF SERVICE

I do hereby certify that a true and correct copy of the foregoing document has been sent to the following counsel of record by E-Mail on May 7, 2009.

/s/ Timothy S. Teter

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